OIPE
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PATENT & TRADEMARK OFFICE

Applicants: Kazi Asaduzzaman et al.
Application No. 10/672,901
Filed: September 26, 2003
For: CLOCK DATA RECOVERY CIRCUITRY AND PHASE LOCKED LOOP CIRCUITRY WITH DYNAMICALLY ADJUSTABLE BANDWIDTHS
Agent: Gall C. Gotfried - Reg. No. 58,333

EXPRESS MAIL LABEL NO. EV620764088US
Docket No.: 174/280 (A1066)
Confirmation No. 9181
Replacement Sheet

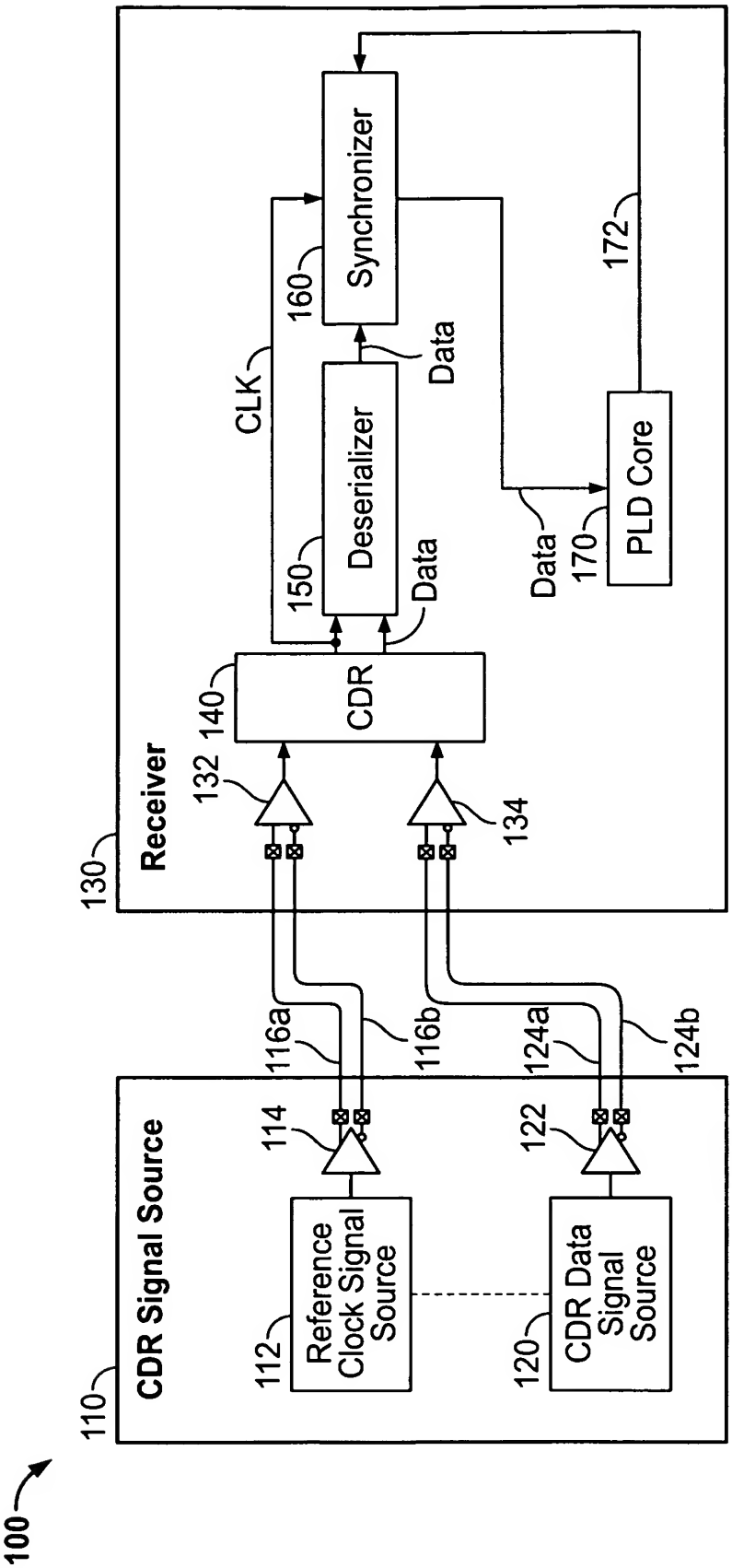

FIG. 1

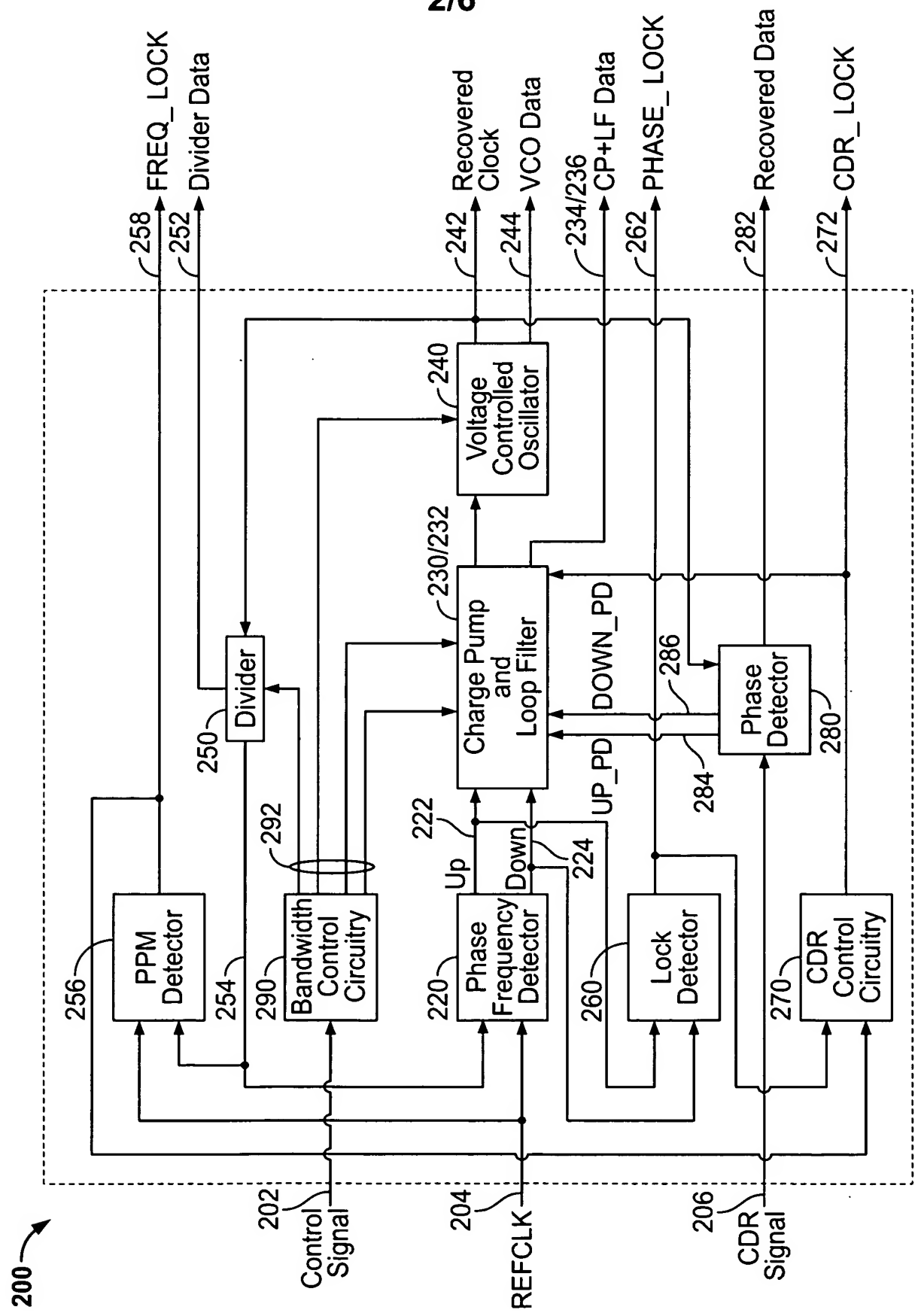
200
202
Control Signal
204
REFCLK
206
CDR Signal
256
PPM Detector
254
290
Bandwidth Control Circuitry
292
220
Phase Frequency Detector
222
Up
Down
224
260
Lock Detector
270
CDR Control Circuitry
250
Divider
230/232
Charge Pump and Loop Filter
UP_PD
DOWN_PD
284
286
280
Phase Detector
240
Voltage Controlled Oscillator
258
FREQ_LOCK
252
Divider Data
242
Recovered Clock
244
VCO Data
234/236
CP+LF Data
262
PHASE_LOCK
282
Recovered Data
272
CDR_LOCK

FIG. 2A

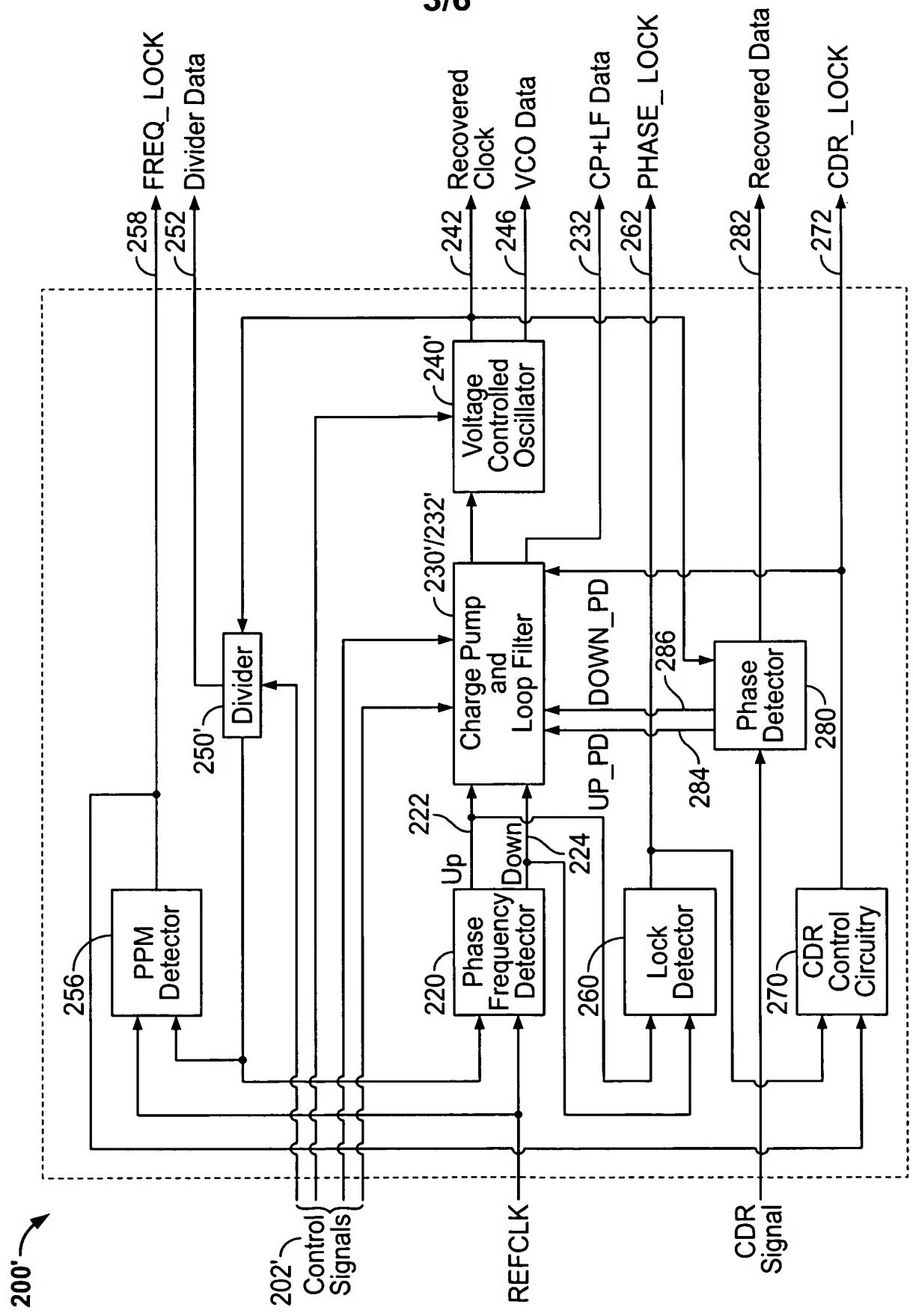
200'
202'
Control Signals
REFCLK
CDR Signal
256
PPM Detector
220
Phase Frequency Detector
260
Lock Detector
270
CDR Control Circuitry
250'
Divider
222
Up
Down
224
UP_PD
DOWN_PD
284
286
230'/232'
Charge Pump and Loop Filter
240'
Voltage Controlled Oscillator
Phase Detector
280
258
FREQ_LOCK
252
Divider Data
242
Recovered Clock
246
VCO Data
232
CP+LF Data
262
PHASE_LOCK
282
Recovered Data
272
CDR_LOCK

FIG. 2B

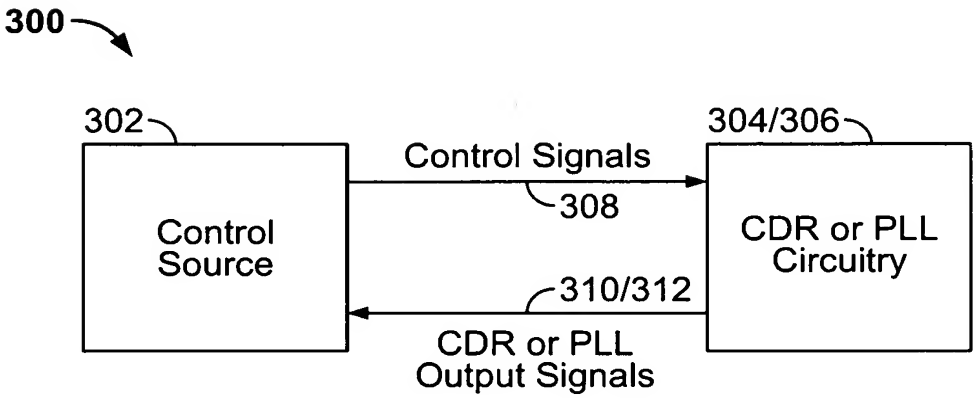
300
302
304/306
Control Signals
308
Control Source
CDR or PLL Circuitry
310/312
CDR or PLL Output Signals

FIG. 3

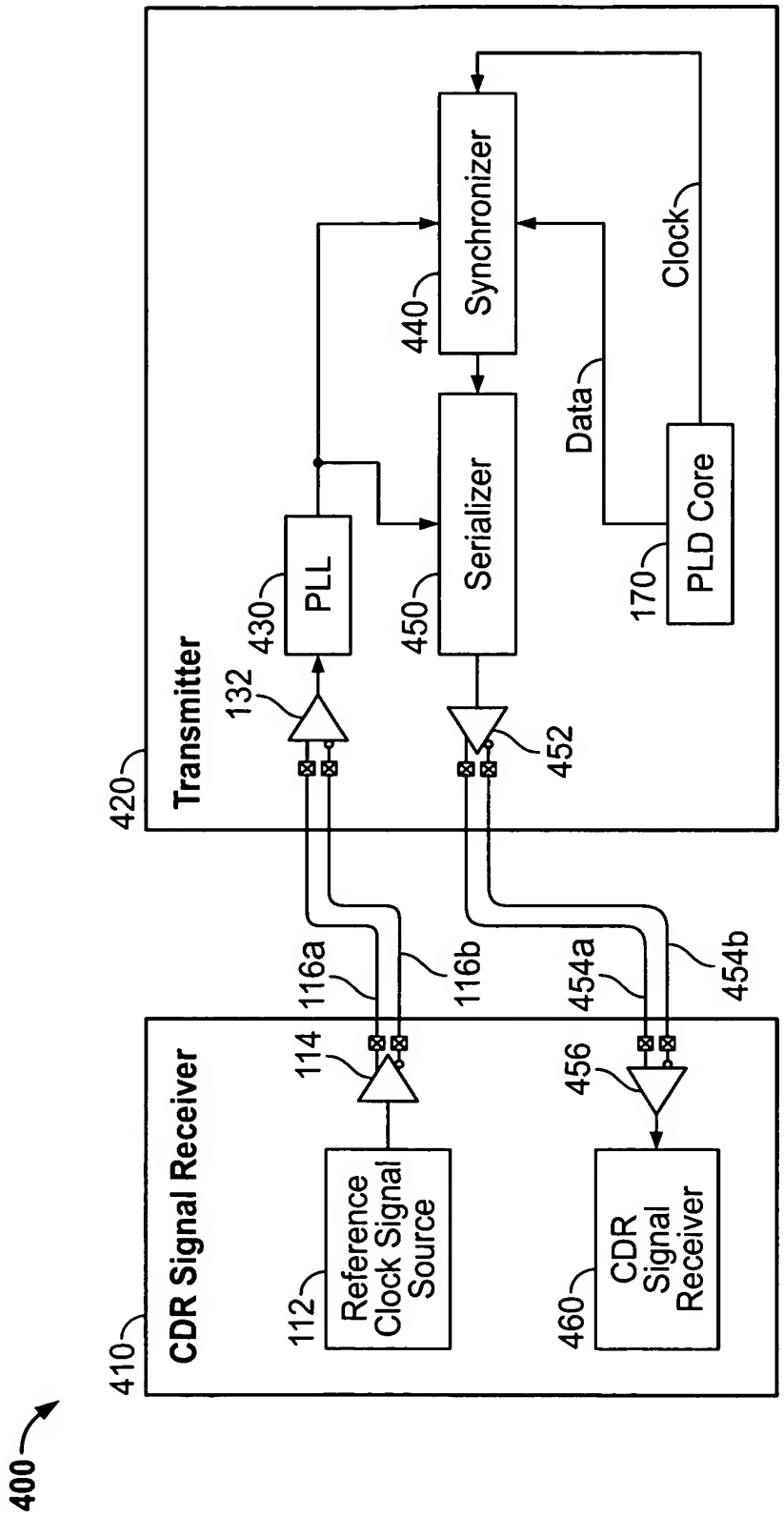
400
410
CDR Signal Receiver
112
Reference Clock Signal Source
114
116a
116b
420
Transmitter
430
PLL
132
440
Synchronizer
450
Serializer
452
454a
454b
456
460
CDR Signal Receiver
170
PLD Core
Data
Clock

FIG. 4

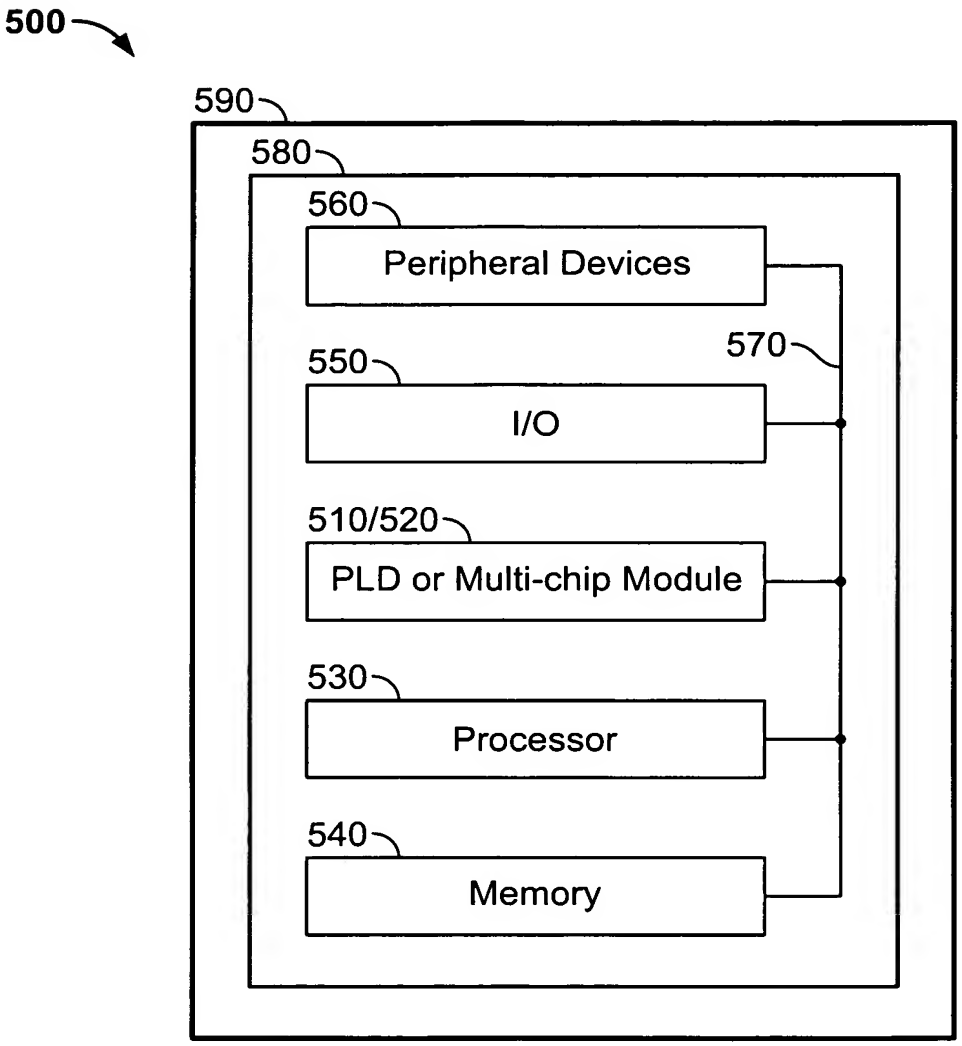
500
590
580
560
Peripheral Devices
570
550
I/O
510/520
PLD or Multi-chip Module
530
Processor
540
Memory

FIG. 5